**CHAPTER 7**

**CONCLUSION**

**7.1 CONCLUSION**

With the aim of achieving low power cache memory, 4T SRAM is chosen. 4T SRAM consumes less power but has more delay when compared to 6T SRAM. Reduction in power is around 30% and increase in delay is 70%. 4T SRAM is used to create a block of cache memory (128 bit) and the maximum access delay of the 4T SRAM cache, which is twice the delay of 6T SRAM, limits the operational frequency. Divided bit line technique is used to decrease the delay and thereby reducing the power-delay product by about 14.56% and 23% in write and read cycles respectively.

**7.2 FUTURE SCOPE**

If a high end tool is used to change the thresholds of load and drive transistors in a 4T cell, a single N-well can be used to accommodate the two PFETS in the cell and an area reduction of 65% of original 6T area can be achieved.

In this project two 4T cells (designed using two N-wells) are merged and reduction in area up to 25% of 6T cell is achieved. If a single N-well is used it may save area up to 50%.

The divided bit line technique applied for a single column in the project. If a high end tool is available it can be applied for the entire array to efficiently reduce dynamic power consumption and delay as well.

If the global bit lines delay is too large, buffers can be used to drive large capacitances and thereby reduce the delay of global bit line.

Row drivers can be used to drive large word line capacitances or two or more row decoders can be used to control word lines from both sides of core and thereby it may reduce delay.